REMARKS

In the Office action, paragraph 1, claims 1-30 stand rejected under 35 U.S.C. § 101 "because the claimed invention is directed to non-statutory subject matter." Claim 1 has been substantially amended. Claims 14-30 have been cancelled without prejudice. Applicant reserves the right to present the subject matter of the cancelled claims for examination in a continuation application at a later date.

Amended claim 1 is the only remaining independent method claim. Claim 1 has been recast as a method of operating an n-dimensional array of processing elements to calculate a global extrema. Claim 1 is comprised of a plurality of steps including serially outputting local extrema from each of a plurality of processing elements to a neighboring processing element until every processing element in a first dimension has received all of the local extrema along a first dimension. A first dimensional extrema is determined and serially output in a manner similar to the manner in which the local extrema is output. The process is repeated for other dimensions until a global extrema is determined. Claim 1 thus recites a plurality of steps for controlling the operation of hardware (processing elements).

The first step in a Section 101 analysis is to determine what the applicant has invented. Here, the applicant has invented and presented in method claim 1 a process. A process defines actions, i.e., a process is an invention that sets forth a series of steps or acts to be performed. In this case, the series of steps or acts are to be performed within an n-dimensional array of processing elements and, more particularly, define the flow of values and the operation of hardware within the array of processing elements. It is respectfully submitted that the subject matter of claim 1 falls within the definition of a process as set forth in 35 U.S.C. § 101. Therefore, that should be the end of the Section 101 analysis. It is not necessary to determine if the subject matter of claim 1 falls within one of the judicial exceptions or admits of a practical application inasmuch as the subject matter, on its face, is a process and therefore statutory.

As further evidence that the claims currently presented are directed to a process and are therefore statutory, the examiner's attention is respectfully directed to the following patents.

U.S. patent no. 5,710,732 is entitled Calculating the Average of Four Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of four unsigned operands, such that the average is an integer rounded away from zero, comprising:

appending two zero's to a left end of each of the operands to provide extended operands;

summing the extended operands to provide an intermediate result;

removing a lowest significant bit and a second lowest significant bit from the intermediate result to provide a shortened intermediate result;

incrementing the shortened intermediate result to provide the average when the removed second lowest significant bit is a one; and

providing the shortened intermediate result as the average when the removed second lowest significant bit is a zero.

U.S. patent no. 5,751,617 is entitled Calculating the Average of Two Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of two unsigned operands such that the average is an integer rounded away from zero in a single instruction cycle, comprising:

logically right-shifting each of the operands by one bit position, wherein bits in a lowest significant bit position of the operands become shifted-out bits;

summing the right-shifted operands to obtain a result; and

incrementing the result when any of the shifted-out bits is a one.

U.S. patent no. 5,835,389 is entitled Calculating the Absolute Difference of Two Integer Numbers in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an absolute difference of first and second unsigned integer operands, such that the absolute difference is an unsigned integer, comprising:

bit-complementing the second operand;

summing the first and bit-complemented second operands to obtain an intermediate result;

incrementing the intermediate result to obtain an incremented intermediate result;

bit-complementing the intermediate result to obtain a bit-complemented intermediate result;

determining whether the intermediate result overflows provided the first and bit-complemented second operands and the intermediate result are considered unsigned numbers;

selecting the incremented intermediate result to obtain the unsigned absolute difference when the overflow occurs; and

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selecting the bit-complemented intermediate result to obtain the unsigned absolute
difference when the overflow does not occur.

U.S. patent no. 5,917,739 is entitled Calculating the Average of Four Integer Numbers Rounded
Towards Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of four signed operands, such that
the average is an integer rounded towards zero in a single instruction cycle, comprising:

appending two bits to a left end of each of the operands to provide extended operands,
wherein for each operand the two appended bits are zero's when the operand is a positive
number, and one's when the operand is a negative number,

summing the extended operands to provide an intermediate result;

removing a lowest significant bit and a second lowest significant bit from the intermediate
result to provide a shortened intermediate result;

incrementing the shortened intermediate result to provide the average when the
intermediate result has a negative value and either of the removed bits is a one; and

providing the shortened intermediate result as the average (i) when the intermediate result
has a positive value, and (ii) when the intermediate result has a negative value and both of
the removed bits are zero's.

U.S. patent no. 6,007,232 is entitled Calculating the Average of Two Integer Numbers Rounded
Towards Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of two unsigned operands such that
the average is an integer rounded towards zero in a single instruction cycle, comprising:

logically right-shifting each of the operands by one bit position, wherein bits in a lowest
significant bit position of the operands become shifted-out bits;

summing the right-shifted operands to obtain a result; and

incrementing the result when both of the shifted-out bits are one's.

New claim 30 is an apparatus claim directed to an n-dimensional array of processing elements
and therefore also falls within the statutory definition of patentable subject matter. See, for example, U.S.
patent no. 7,031,996 entitled Calculating Square Root of Binary Numbers with Fixed-Point
Microprocessor. Claim 1 provides:

1. A square root calculator comprising:

a binary searching module operable to accept a number, perform a binary search

operation, and return an integer portion of the square root of the number;

a fraction calculating module operable to calculate a fractional portion of the square root;

and a summing module operable to sum the integer portion and the fractional portion to

obtain the square root.

Finally, applicant asserts that the method of claim 1 and the apparatus of claim 30 are no

different in principle from methods and apparatus for generating random numbers. It could be

argued that random numbers not applied to a specific problem do not represent anything in the

real world, yet the Office routinely grants patents containing method and apparatus claims that do

no more than generate random numbers. The following represents but a small sample of the

hundreds of such patents routinely granted that recite either a process, an apparatus, or both, for

generating random numbers:

7,233,965	Continuous Random Number Generation Method and Apparatus June 19, 2007
7,197,523	Efficient Use of Detectors for Random Number Generation March 27, 2007
7,188,131	Random Number Generator March 6, 2007
7,176,882	True Random Number Generation January 23, 2007

In view of the foregoing, it is believed that the 35 U.S.C. § 101 rejection in the last Office action

has been overcome and should now be withdrawn.

In the last Office action, paragraph 2, claims 1-30 were provisionally rejected under the judicially

created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 31 of

copending application no. 10/689,449 and claims 14-21 were provisionally rejected as being unpatentable

over claims 14-21 and 38-30 of copending Application No. 10/689,335. Because this is a provisional

obviousness-type double patenting rejection, the double patenting rejection will be addressed at such time

as allowable subject matter is indicated in the instant application.

Request for Interview

Applicant has made a diligent effort to place the instant application in condition for allowance. If

the examiner is of the opinion that the instant application is in condition for disposition other than through

allowance, the examiner is respectfully requested to contact applicant's attorney at the telephone number

listed below **so that an interview may be scheduled before the issuance of a first Office action rejection**.

Respectfully submitted,

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